ESD Association Technical Report

ESD TR5.4-04-13

For Electrostatic Discharge Sensitivity Testing

Transient Latch-up Testing

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Working Group 5.4,

Transient Latch-up

ESD Association

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FOREWORD

At the time the ESD TR5.4-04-13 was prepared, the 5.4 Device Testing (TLU) subcommittee had the following members:

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1.0 INTRODUCTION

1.1 Definition

Transient latch-up (TLU) is defined as a state in which a low-impedance path, resulting from a transient overstress that triggers a parasitic thyristor structure or bipolar structure or combinations of both, persists at least temporarily after removal or cessation of the triggering condition. The rise time of the transient overstress causing TLU is shorter than five µs.[1]

TLU as defined in this document does not cover changes of functional states, even if those changes would result in a low-impedance path and increased power supply consumption.

1.2 History

Latch-up, sometimes called bipolar latch-up, in integrated circuits is a condition in which an unexpected voltage or current triggers a high current condition, which continues even when the trigger signal is removed. Ending a latch-up condition requires the removal of power from the integrated circuit. Latch-up occurs primarily in CMOS integrated circuits and variations on this technology such as BiCMOS. Since electrical systems containing latch-up sensitive integrated circuits could be unreliable, integrated circuits should be tested for their immunity to latch-up. The most commonly used latch-up test, JEDEC JESD78 [1], attempts to trigger latch-up using relatively long duration and slowly rising voltage and current triggers. JEDEC JESD78 is successful at detecting integrated circuits with serious latch-up immunity issues. The success of JEDEC JESD78 in detecting latch-up advances in the understanding of latch-up and improved design techniques has made latch-up a relatively rare failure mechanism. However, latch-up failures still occur, often in integrated circuits which show no latch-up sensitivity when tested with JEDEC JESD78. The trigger for latch-up in these situations is often found to be very fast transients, either on input or output circuits or power supplies. This type of latch-up has been called transient latch-up. The failure of JEDEC JESD78 to detect these types of latch-up and the disruption and cost of transient latch-up failures has resulted in requests for a standardized transient latch-up test method to detect latch-up sensitivity earlier in the design cycle. There is unfortunately no agreement on what a transient latch-up test method should be. There is no agreement on the stress waveform, if the stress should be voltage or current or even if the stress should be applied to signal pins or to power supply rails. A first attempt at a transient latch-up test method, ESDA SP5.4-2008, was not widely adopted by the industry for reasons to be discussed below. Faced with this situation, ESDA WG 5.4 decided to write a technical report (TR) which would provide a comprehensive summary of the state of transient latch-up. It was hoped that by compiling a summary of the state of knowledge on the subject, it would make it clear whether a single transient latch-up test was needed or if a small set of stress tests could cover a large fraction of the integrated circuits which have latch-up sensitivity when exposed to transient signals.

This TR consists of five technical sections and list of references. This introduction section includes the motivation for the technical report. In addition, a high level explanation of latch-up, followed by a review of existing latch-up test methods and their limitations, including JEDEC JESD78 and similar “DC” latch-up tests, the transient latch-up test from WG 5.4 and the “Panasonic” test. Section 2.0 is a brief overview of previous work published in literature. Section 3.0 gives a more thorough treatment of the phenomenon of transient latch-up. Section 4.0 contains descriptions of latch-up case histories and tests categorized by application area, including digital ICs, wireless communication, automotive, high voltage applications, and audio. Section 5.0 provides a summary and conclusions.

[1] Five µs is the minimum rise time of “static” latch-up according to JEDEC JESD78D. The trigger pulse width is unspecified, it can be in the range of JEDEC JESD78D range (> 2 × t_{rise}) or shorter.