

***ESD TR5.4-04-13***

# ***ESD Association Technical Report***

***ESD TR5.4-04-13***

***For Electrostatic Discharge  
Sensitivity Testing***

***Transient Latch-up Testing***

***Authors:***  
**Working Group 5.4,**  
**Transient Latch-up**  
ESD Association



*Electrostatic Discharge Association*  
7900 Turin Rd., Bldg. 3  
Rome, NY 13440

---

**CAUTION  
NOTICE**

---

Electrostatic Discharge Association (ESDA) standards and publications are designed to serve the public interest by eliminating misunderstandings between manufacturers and purchasers, facilitating the interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining the proper product for his particular needs. The existence of such standards and publications shall not, in any respect, preclude any member or non-member of the Association from manufacturing or selling products not conforming to such standards and publications. Nor shall the fact that a standard or publication is published by the Association preclude its voluntary use by non-members of the Association, whether the document is to be used domestically or internationally. Recommended standards and publications are adopted by the ESDA in accordance with the ANSI Patent policy.

Interpretation of ESDA Standards: The interpretation of standards, in-so-far as it may relate to a specific product or manufacturer, is a proper matter for the individual company concerned and cannot be undertaken by any person acting for the ESDA. The ESDA Standards Chairman may make comments limited to an explanation or clarification of the technical language or provisions in a standard, but not related to its application to specific products and manufacturers. No other person is authorized to comment on behalf of the ESDA on any ESDA Standard.

---

**DISCLAIMER OF  
WARRANTIES**

---

THE CONTENTS OF ESDA'S STANDARDS AND PUBLICATIONS ARE PROVIDED "AS-IS," AND ESDA MAKES NO REPRESENTATIONS OR WARRANTIES, EXPRESSED OR IMPLIED, OF ANY KIND WITH RESPECT TO SUCH CONTENTS. ESDA DISCLAIMS ALL REPRESENTATIONS AND WARRANTIES, INCLUDING WITHOUT LIMITATION, WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR USE, TITLE, AND NON-INFRINGEMENT.

---

**DISCLAIMER OF  
GUARANTY**

---

ESDA STANDARDS AND PUBLICATIONS ARE CONSIDERED TECHNICALLY SOUND AT THE TIME THEY ARE APPROVED FOR PUBLICATION. THEY ARE NOT A SUBSTITUTE FOR A PRODUCT SELLER'S OR USER'S OWN JUDGEMENT WITH RESPECT TO ANY PARTICULAR PRODUCT DISCUSSED, AND ESDA DOES NOT UNDERTAKE TO GUARANTEE THE PERFORMANCE OF ANY INDIVIDUAL MANUFACTURERS' PRODUCTS BY VIRTUE OF SUCH STANDARDS OR PUBLICATIONS. THUS, ESDA EXPRESSLY DISCLAIMS ANY RESPONSIBILITY FOR DAMAGES ARISING FROM THE USE, APPLICATION, OR RELIANCE BY OTHERS ON THE INFORMATION CONTAINED IN THESE STANDARDS OR PUBLICATIONS.

---

**LIMITATION ON  
ESDA's LIABILITY**

---

NEITHER ESDA, NOR ITS MEMBERS, OFFICERS, EMPLOYEES, OR OTHER REPRESENTATIVES WILL BE LIABLE FOR DAMAGES ARISING OUT OF, OR IN CONNECTION WITH, THE USE OR MISUSE OF ESDA STANDARDS OR PUBLICATIONS, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. THIS IS A COMPREHENSIVE LIMITATION OF LIABILITY THAT APPLIES TO ALL DAMAGES OF ANY KIND, INCLUDING WITHOUT LIMITATION, LOSS OF DATA, INCOME, OR PROFIT, LOSS OF OR DAMAGE TO PROPERTY AND CLAIMS OF THIRD PARTIES.

Published by:

**Electrostatic Discharge Association**  
**7900 Turin Road, Bldg. 3**  
**Rome, NY 13440**

Copyright © 2013 by ESD Association  
All rights reserved

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Printed in the United States of America

## FOREWORD

At the time the ESD TR5.4-04-13 was prepared, the 5.4 Device Testing (TLU) subcommittee had the following members:

Wolfgang Stadler, Chair Intel Mobile Communications		
Robert Ashton ON Semiconductor	Lorenzo Cerati STMicroelectronics	Marcel Dekker MASER Engineering BV
Marti Farris Intel Corporation	Reinhold Gaertner Infineon Technologies	Robert Gauthier IBM
Horst Gieser Fraunhofer EFMT	Vaughn Gross Green Mountain ESD Labs, LLC	Evan Grund Grund Technical Solutions, LLC
Leo G. Henry ESDTLP Consultants	Tom Meuse Thermo Fisher Scientific	Kathy Muhonen RF Micro Devices
Nate Peachey RF Micro Devices	Bill Reynolds IBM	Alan Righter Analog Devices
Masanori Sawada Hanwa Electronic Ind. Co., Ltd.	Mirko Scholz IMEC	Theo Smedes NXP Semiconductors
Steven Voldman Dr. Steven H. Voldman, LLC		Scott Ward Texas Instruments, Inc.

The following individuals made significant contributions to ESD TR5.4-03-13:

Krzysztof Domanski Infineon Technologies	Wolfgang Reinprecht ams AG
---------------------------------------------	-------------------------------

## TABLE OF CONTENTS

<b>1.0 INTRODUCTION .....</b>	<b>1</b>
1.1 DEFINITION .....	1
1.2 HISTORY .....	1
1.3 LATCH-UP FUNDAMENTALS .....	2
1.4 LATCH-UP TEST METHODS.....	3
1.4.1 JEDEC JESD78 Style Tests .....	3
1.4.2 An Attempt at Transient Latch-up Test Method – ANSI ESD SP5.4-2008 (now ESD TR5.4-03-11) .....	4
1.4.3 Panasonic “Machine Model” Transient Latch-up Method .....	5
<b>2.0 LITERATURE AND PREVIOUS WORK ON TLU .....</b>	<b>8</b>
<b>3.0 GENERAL OVERVIEW OF THE TLU PHENOMENON.....</b>	<b>9</b>
3.1 INTERNAL TLU .....	9
3.1.1 Internal TLU during Supply Test (Overvoltage Stress).....	11
3.1.2 Internal TLU during IO Test (Current Injection) .....	12
3.1.3 Internal TLU during ANSI/ESD SP5.4 (ESD TR5.4-03-11) Test (Supply Undershoot).....	14
3.1.4 Temperature Dependence in Internal TLU Phenomenon.....	15
3.2 EXTERNAL TLU .....	15
3.2.1 Trigger Pulse Slew-Rate in External TLU Phenomenon.....	17
3.2.2 Pulse Width Dependency in External TLU Phenomenon .....	20
3.2.3 External TLU Due to Bipolar Injection.....	22
3.2.4 Temperature Dependency in External TLU Phenomenon.....	22
<b>4.0 APPLICATION AREAS.....</b>	<b>23</b>
4.1 DIGITAL AND HIGH-SPEED ICs (MICROPROCESSORS).....	23
4.1.1 General Description of Possible TLU Threats in Digital and High-Speed ICs.....	23
4.1.2 Examples .....	23
4.1.3 Possible Test Methods to Reproduce these Examples .....	27
4.2 (WIRELESS) COMMUNICATION .....	27
4.2.1 General Description of Possible TLU Threats in (Wireless) Communication Applications.....	27
4.2.2 Examples .....	27
4.2.3 Possible Test Methods to Reproduce these Examples .....	36
4.3 AUTOMOTIVE .....	37
4.3.1 General Description of Possible TLU Threats in Automotive Applications.....	37
4.3.2 Examples .....	37
4.3.3 Possible Test Methods to Reproduce these Examples .....	40
4.4 HIGH-VOLTAGE APPLICATIONS (NON-AUTOMOTIVE) .....	41
4.4.1 General Description of Possible TLU Threats in High-Voltage Applications .....	41
4.4.2 Examples .....	41

4.4.3 Possible Test Methods to Reproduce these Examples .....	47
4.5 LATCH-UP IN ANALOG DESIGN .....	48
4.5.1 Introduction .....	48
4.5.2 Examples .....	50
4.5.3 Possible Test Methods to Reproduce these Examples .....	54
<b>5.0 SUMMARY AND CONCLUSION .....</b>	<b>54</b>
5.1 CATEGORIES OF TLU FAILS AND TLU TESTS TO REPRODUCE THE FAILS .....	54
5.2 RECOMMENDATIONS FOR NEXT STEPS TOWARDS STANDARDIZATION OF TLU TEST METHODS .....	56
<b>6.0 BIBLIOGRAPHY .....</b>	<b>57</b>

## TABLES

Table 1: Timing Parameters of Voltage and Current Stresses .....	3
Table 2: Parameters for ESD TR5.4-03-11 (ANSI/ESD SP5.4-2008) Stress Pulse .....	4
Table 3: Summary Table of MM TLU Pin / Power Supply Requirements and Failure Criteria .....	8
Table 4: Compilation of Possible Test Methods to Reproduce the Examples Discussed in Section 4.1.2 .....	27
Table 5: Latch-up Withstand Currents of Different Trigger Pulses (Static LU, Transient LU, and CDE) at 100 °C .....	36
Table 6: Compilation of Possible Test Methods to Reproduce the Examples Discussed in Section 4.2.2 .....	37
Table 7: Compilation of Possible Test Methods to Reproduce the Examples Discussed in Section 4.3.2 .....	40
Table 8: Compilation of Possible Test Methods to Reproduce the Examples Discussed in Section 4.4.2 .....	47
Table 9: Compilation of Possible Test Methods to Reproduce the Examples Discussed in Section 4.5.2 .....	54

## FIGURES

Figure 1: Cross Section of Basic CMOS Structure Showing Parasitic Bipolar Transistors and Substrate and Well Resistances .....	2
Figure 1: I/V Curve of a Latch-up Showing Normal Low Current and Latch-up States .....	3
Figure 3: Transient Latch-up Pulse from ESD TR5.4-03-11 (ANSI/ESD SP5.4-2008) .....	4
Figure 4: MM TLU Test Setup Diagram .....	6
Figure 5: ESD Test System / Power Supply / Oscilloscope Setup for MM Transient Latch-up ...	6
Figure 6: Equivalent Circuit of an Example ESD Power-Clamp Which is Sensitive to Certain Slew-Rate .....	11
Figure 7: I/V of Power-Clamp from Figure 6, Comparison of TLP ( $dV/dt < 0.1$ volts/ns) to DC ( $dV/dt > 1$ volts/ $\mu$ s) .....	12
Figure 8: Cross-Section of a Typical CMOS Output Driver Stage .....	12
Figure 9: A Plot of TLU Trigger Current versus Pulse Rise Time for a Typical Parasitic SCR in CMOS Technology .....	13
Figure 10: TLU Trigger Current versus Pulse Width for a Typical Parasitic SCR in CMOS Technology .....	14
Figure 11: Cross-Section of Two Inverters at Different Supply Voltage VDD1 and VDD2 .....	15
Figure 12: Cross Section of an Arbitrary Region of the IC Containing a Critical Parasitic SCR, GR, and Injection Source .....	16
Figure 13: Equivalent Circuit of the DC/DC Converter Which Contains an External Coil .....	17

Figure 14: Voltage Drop at the Parasitic SCR during the External TLU Current Injection to the $n+$ Diffusion.....	18
Figure 15: Topology of the IO Test Chip Which was used for the TLU Tests, a Negative TLU Injection was Performed to the IO7, TLU Occurred at VDDP .....	19
Figure 16: TLU Trigger Current of Two Samples (#42, #49) at IO7 versus: a) Pulse Fall Time, Rising Edge was Kept at 10 $\mu$ s; b) Pulse Rise Time, Falling Edge was Kept at 10 $\mu$ s.....	19
Figure 17: External TLU Trigger Current versus Trigger Pulse Width [10] for Negative Currents Injected to $n+/p$ -well Diode .....	20
Figure 18: External TLU Trigger Current versus Trigger Pulse Width [8] for Positive Current Injection to $p+/n$ -well Diode .....	21
Figure 19: External TLU Trigger Current in Different Temperatures .....	22
Figure 20: Schematic of Power Array and ESD Clamp; Layout of Power Array and ESD Clamp .....	23
Figure 21: 10 ns TLP Characteristics Comparison between Stand-Alone ESD Clamp and ESD Clamp with Gate (Vin) Bias Variation.....	24
Figure 22: Different Power-Rail ESD Clamp Circuits Designed with (A) Typical RC-Based Detection, (B) NMOS and PMOS Feedback, (C) PMOS Feedback, and (D) Cascaded PMOS Feedback.....	25
Figure 23: Measured VDD and IDD Waveforms on the Power-Rail ESD Clamp Circuit with NMOS and PMOS Feedback under System-Level ESD Test with ESD Voltage of - 200 Volts.....	25
Figure 24: Measurement Set-up of the System-Level ESD Test with Indirect Contact-Discharge Test Mode.....	26
Figure 25: Measured VDD Transient Waveform of One (CMOS IC #1) of the CMOS ICs Inside the EUT with an ESD Voltage of -1000 Volts Zapping on the HCP.....	26
Figure 26: Modified Component-Level TLU Measurement Set-up with Bipolar Trigger.....	26
Figure 27: DC /V Characteristics of the Diode Triggered SCR Power Clamp.....	28
Figure 28: EMMI Snapshot of the Power Clamp after EOS Stress .....	28
Figure 29: Part of the Core Circuitry Which has Involved Sensitive Parasitic SCR .....	29
Figure 30: Topology of the External Connection Which Revealed Susceptibility to TLU, but Could not Produce LU during the Standard JEDEC LU Test.....	30
Figure 31: EMMI Snapshot of the Parasitic Thyristor after the Displacement Current Injection through the CAP at Plug .....	30
Figure 32: ESD Protection Scheme of the USB Pad .....	31
Figure 33: Layout of the IO Pad and ESD Devices .....	31
Figure 34: Measurement at IO with Connected VDD 2.8 Volts .....	32
Figure 35: Measurement at IO with Disconnected VDD 2.8 Volts.....	32
Figure 36: After the Injection of - 40 milliamperes (Pulse Width = 10 ms), the Current is Observed at VDDP for Approximately 50 ms .....	33
Figure 37: TIVA (Thermally Induced Voltage Alternation) Measurement of the Chip Reveals Circuitry which is Sensitive to the Substrate Current .....	34
Figure 38: Topology of the Circuit which is Sensitive to the Negative Current Injection .....	34
Figure 39: CDE Waveform for 10 m, 20 m, and 40 m Long Cables after they are Charged with Voltages Corresponding to the CDE / TLU trigger Threshold of TC2_IO1 .....	35
Figure 40: TLU Threshold Trigger Current (Negative Polarity) of IO1 Pin of TC2 versus Duration of the Trigger Pulse (81104A, $t_r$ = 10 ns) at 100 °C Ambient Temperature .	36
Figure 41: Bond Wire Damages on an Automotive Power Device due to TLU .....	38
Figure 42: Emission Microscope Spot Showing the Trigger Mechanism .....	38
Figure 43: Diagram of an IC in an Automotive Application Which Latched up during an EOS Test on Supply Pin UBAT .....	39
Figure 44: Due to the EOS Overvoltage at the Supply, the Parasitic NPN was Triggered that Caused a Permanent Current Is to Flow on the Supply .....	39
Figure 45: Parasitic Structure in the Chip .....	40
Figure 46: Cross Section of the Parasitic npn Which was Triggered in Result of the EOS Test in a Car .....	40

---

Figure 47: PFA Picture of the High Voltage Power Clamp of XDSL IC Product and Schematics .....	42
Figure 48: Electrical Characterization of the HV SCR Power Clamp .....	42
Figure 49: Transient Latch-up Analysis of XDSL IC at Supply Line .....	43
Figure 50: Couple of Cells within the Digital Part Latch; Zoomed Section of TLU .....	43
Figure 51: Scope Views of TLU Event.....	44
Figure 52: EOS on Returned Part Inside VSS Pad; EOS Hard Latch-up at Metal and LDO .....	45
Figure 53: Soft Latch-up Condition (LDO); Soft Latch-up Condition (LV Part).....	45
Figure 54: Scope View Showing the Voltage Ringing on VDD_HV after the Latch-up Load on the LV-I/O Causing the Instability of the LDO .....	46
Figure 55: Trigger Current during Positive Event; Circuit in Latch Condition .....	46
Figure 56: EOS Fail Inside RC Clamp; Simulated TLU .....	47
Figure 57: Analog I/O P-Channel MOSFET EMMI Photon Emissions .....	49
Figure 58: Analog I/O Latch-up between PFET Pull-up and Adjacent Decoupling Capacitors ....	50
Figure 59: Power Management Product Output Driver Weakness due to Transient Latch-up ....	50
Figure 60: Shoot through Caused by Glitch on SW1 Causing Bounce on PGND and PVIN .....	51
Figure 61: DC-DC Converter Failure of the NMOS Output Driver Circuit.....	51
Figure 62: Audio Output Driver Application .....	52
Figure 63: PC Audio Short Circuit Test Setup .....	52
Figure 64: Measurement Detail of Activating Short Circuit Protection with Current below Level Which Would Result in MN1 Damage (ORNF Ringing but Staying Stable) .....	53
Figure 65: Measurement Detail of Activating Short Circuit Protection Resulting in MN1 Damage (ORNF Failing).....	54





---

**ESD Association Technical Report For Electrostatic Discharge Sensitivity Testing - Transient Latch-up Testing**

---

**1.0 INTRODUCTION****1.1 Definition**

Transient latch-up (TLU) is defined as a state in which a low-impedance path, resulting from a transient overstress that triggers a parasitic thyristor structure or bipolar structure or combinations of both, persists at least temporarily after removal or cessation of the triggering condition. The rise time of the transient overstress causing TLU is shorter than five  $\mu\text{s}$ .<sup>1</sup>

TLU as defined in this document does not cover changes of functional states, even if those changes would result in a low-impedance path and increased power supply consumption.

**1.2 History**

Latch-up, sometimes called bipolar latch-up, in integrated circuits is a condition in which an unexpected voltage or current triggers a high current condition, which continues even when the trigger signal is removed. Ending a latch-up condition requires the removal of power from the integrated circuit. Latch-up occurs primarily in CMOS integrated circuits and variations on this technology such as BiCMOS. Since electrical systems containing latch-up sensitive integrated circuits could be unreliable, integrated circuits should be tested for their immunity to latch-up. The most commonly used latch-up test, JEDEC JESD78 [1], attempts to trigger latch-up using relatively long duration and slowly rising voltage and current triggers. JEDEC JESD78 is successful at detecting integrated circuits with serious latch-up immunity issues. The success of JEDEC JESD78 in detecting latch-up advances in the understanding of latch-up and improved design techniques has made latch-up a relatively rare failure mechanism. However, latch-up failures still occur, often in integrated circuits which show no latch-up sensitivity when tested with JEDEC JESD78. The trigger for latch-up in these situations is often found to be very fast transients, either on input or output circuits or power supplies. This type of latch-up has been called transient latch-up. The failure of JEDEC JESD78 to detect these types of latch-up and the disruption and cost of transient latch-up failures has resulted in requests for a standardized transient latch-up test method to detect latch-up sensitivity earlier in the design cycle. There is unfortunately no agreement on what a transient latch-up test method should be. There is no agreement on the stress waveform, if the stress should be voltage or current or even if the stress should be applied to signal pins or to power supply rails. A first attempt at a transient latch-up test method, ESDA SP5.4-2008, was not widely adopted by the industry for reasons to be discussed below. Faced with this situation, ESDA WG 5.4 decided to write a technical report (TR) which would provide a comprehensive summary of the state of transient latch-up. It was hoped that by compiling a summary of the state of knowledge on the subject, it would make it clear whether a single transient latch-up test was needed or if a small set of stress tests could cover a large fraction of the integrated circuits which have latch-up sensitivity when exposed to transient signals.

This TR consists of five technical sections and list of references. This introduction section includes the motivation for the technical report. In addition, a high level explanation of latch-up, followed by a review of existing latch-up test methods and their limitations, including JEDEC JESD78 and similar "DC" latch-up tests, the transient latch-up test from WG 5.4 and the "Panasonic" test. Section 2.0 is a brief overview of previous work published in literature. Section 3.0 gives a more thorough treatment of the phenomenon of transient latch-up. Section 4.0 contains descriptions of latch-up case histories and tests categorized by application area, including digital ICs, wireless communication, automotive, high voltage applications, and audio. Section 5.0 provides a summary and conclusions.

---

<sup>1</sup> Five  $\mu\text{s}$  is the minimum rise time of "static" latch-up according to JEDEC JESD78D. The trigger pulse width is unspecified, it can be in the range of JEDEC JESD78D range ( $> 2 \times t_{\text{rise}}$ ) or shorter.