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IEEE Standard Format for LSI-Package-Board Interoperable Design

IEEE Computer Society

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IEEE Standard Format for LSI-Package-Board Interoperable Design

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Abstract: A method is provided for specifying a common interoperable format for electronic systems design. The format provides a common way to specify information/data about the project management, netlists, components, design rules, and geometries used in Large-Scale Integrated Circuit-Package-Board designs. The method provides the ability to make electronic systems a key consideration early in the design process; design tools can use it to exchange information/data seamlessly.

Keywords: common interoperable format, components, design analysis, design rules, geometries, IEEE 2401™, large-scale integrated circuits, netlists, packages for LSI circuits, printed circuit board, project management, Verilog-HDL

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The following members of the entity balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Cadence Design Systems, Inc.
Japan Electronics and Information Technology Industries Association (JEITA)
Marvell Semiconductor, Inc.
Synopsys, Inc.
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Introduction

This introduction is not part of IEEE Std 2401™-2015, IEEE Standard Format for LSI-Package-Board Interoperable Design.

To deal with the increasing difficulty of design and the cost competitiveness of the global market, and to shorten the development term, innovative design methodologies should be implemented. It has been difficult to achieve the optimization of an entire set of large-scale integrated (LSI) circuits, packages, and board (LPB) using individual design processes for each LPB part.

One possibility for optimization is to have a certain section design the whole LPB; however, gathering knowledge and integrating the design environment of each LPB part is difficult. Dedicated professional technicians of individual LPB parts, who have the best knowledge and performance of their own part's design tools, intend to create design optimization by having proper interoperable information exchanges among all LPB parties. In order to achieve a design that optimizes the balance between cost and performance, information about and the results of design should be well shared among cooperating LPB design sections.

The Japan Electronics and Information Technology Industries Association (JEITA) LPB Interoperable Design Process Working Group (LPB-WG) was established to identify the solution. The LPB-WG intends to make a standard for an exchange format to make it easy to exchange information between each of the LPB design departments, so that optimal design will be carried out quickly.

The LPB interoperable design process has the following issues:

- Netlist not unified on each LPB
- Complexity of the representation of the relationship as a whole arrangement of the LPB
- Differences in how to give the design constraints, lack of design information, and many discrepancies in design rules.
- Databases not unified in each LPB, or among different vendors
- No unified terms

Various problems caused by these issues include the following:

- A large effort is required for conversion of formats.
- The occurrence of conversion errors and connection errors is difficult to detect because there is a lack of the information needed to do so.
- It takes a long time to gather information, resulting in a long period of design and analysis.
- It is difficult to make optimal design changes because the entire verification process is difficult.
- EDA tool cost increase because of additional development required to support multiple formats.
- It is time-consuming for designers to communicate their intentions in a way that others understand.

Based on this analysis, the LPB-WG has established an interface format that can address these issues.

As the one of the case studies of the LPB interoperable design process, the power distribution network (PDN) should be designed with information about the other LPB parts to reduce the noise (see Figure i).

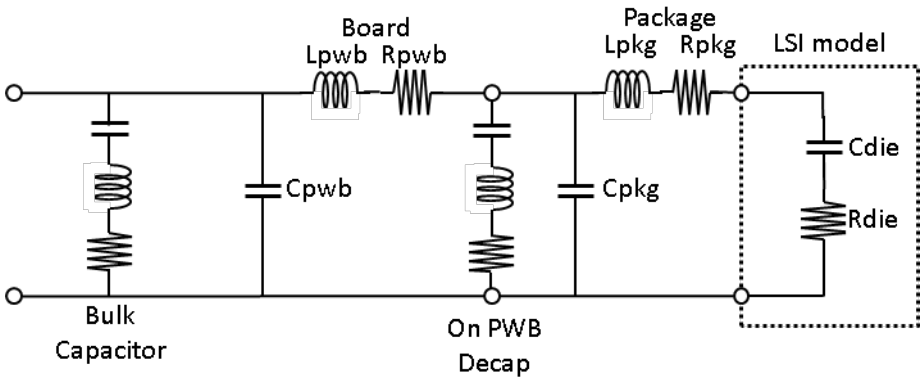

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Figure i—Power distribution network

Resonance is caused by a capacitance and inductance present in the various parts in the LPB PDN. Impedance at the resonant frequency will be extremely large. If each part of the overall LPB design is not accurately simulated in the PDN model, the power supply circuit cannot be correctly designed (see Figure ii).

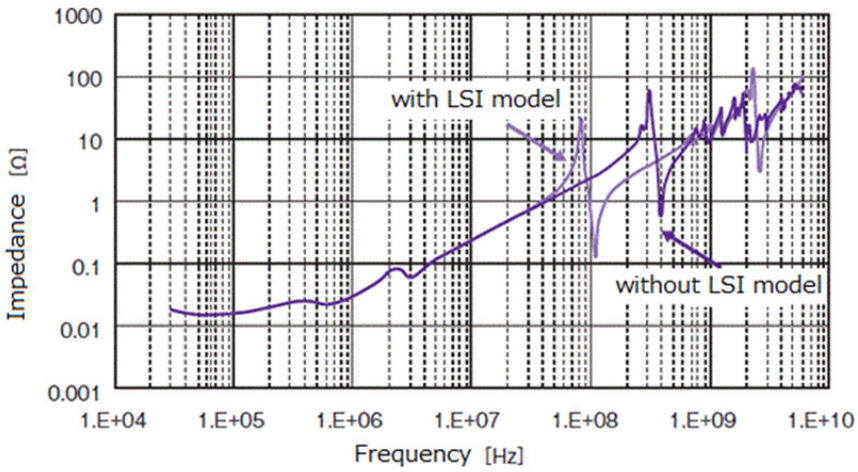

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Figure ii—Example of PDN impedance

In order to run properly, this simulation should align a variety of information, such as the circuit model of power distribution network (PDN) of LSI, shape information about the package and board, electrical parameters of materials, and models of the components. It is difficult to make an efficient design when the specification or format of the design information is different in each part of the LPB, and the necessary parameters are not shared. When the format of the interface methods and models of the simulation are not consistent, the setup time and the cost of design/verification are enormous, which has become a barrier to cooperation in LPB design. The LPB-WG was established in JEITA to explore ways to create a mutual LPB interface to enable a more efficient co-design environment.

Contents

IEEE Standard Format for LSI-Package-Board Interoperable Design

1. Overview

1.1 Scope

This standard defines a common interoperable format that will be used for the design of a) large-scale integration (LSI), b) packages for such LSI, and c) printed circuit boards on which the packaged LSI are interconnected. Collectively, such designs are referred to as" LSI-Package-Board" (LPB) designs. The format provides a common way to specify information/data about the project management, netlists, components, design rules, and geometries used in LPB designs.

1.2 Purpose

The general purpose of this standard is to develop a common format that LPB design tools can use to exchange information/data seamlessly, as opposed to having to work with multiple different input and output formats.

1.3 Key characteristics of the LSI-Package-Board Format

LPB format will facilitate the exchange of design information. This functionality provides the ability to plan the entire design at an early stage. In effect, post-design analysis will be possible throughout the entire